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Transferred Electron Logic Devices for Gigabit-Rate Signal Processing

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***Abstract*—A new approach for designing transferred electron logic devices (TELD's) is presented and experimental results described. Electrolytic thinning of GaAs wafers has been used to maintain uniform *nd* product across the wafers and minimize variations in the device characteristics. TELD's have been fabricated and their performance studied. The devices are evaluated as threshold logic elements. The parameters studied are 1) switching characteristics, 2) shortest pulses that can be processed, and 3) device delay and dissipation. Experimentally, pulses as small as 80 ps wide have been processed through transferred electron logic gates (TELG's) with device delays of the order of 50 ps and delay–dissipation product of 5–10 pJ, which make them suitable for gigabit-rate signal processing.**

List of Symbols

A	Cross-sectional area of the test Schottky diodes.
c	Input capacitance of a TELD + capacitance of the interconnecting lines.
d	Active layer (channel) thickness.
e	Electronic charge.
E	Electric field.
g_m	Transconductance below threshold field.
G_v	Voltage gain.
I	Device current.
I_{th}	Device threshold current.
l_c	Distance between the cathode and gate.
l_{ca}	Distance between cathode and anode.
l_g	Gate length.
l_t	Distance between the gate and anode (transit length).
n	Doping density.
Q	Total charge.
R_L	Load resistance.
S	Device cross-sectional area ($= Wd$).
V_o	Output voltage developed across the load resistor due to the signal present at the gate.
W	Width of the active layer.
$x_{1th}x_{2th}$	Depletion layer thickness at the anode and cathode edge of the gate, respectively, normalized to the channel thickness.
ΔI	Current dropback when the device thresholds.
ΔV_g	Trigger signal at the gate.
σ	Electrical conductivity.
μ	Electron mobility.
ϕ	Voltage drop across the depletion layer at the anode edge of the gate.
ϕ_b	Built-in diffusion potential.
ϕ_p	Channel pinchoff voltage.
τ_D	Propagation delay.

Manuscript received May 13, 1976; revised July 26, 1976. This work was supported by the Office of Naval Research, Arlington, VA, under Contract N00014-75-C-0100.

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I. Introduction

In the last few years, the feasibility of using the transferred electron effect in GaAs to develop gigabit-rate threshold logic elements has been demonstrated. Several researchers [1]-[4] have developed planar Schottky-barrier gate transferred electron logic devices (TELD's) and demonstrated that propagation delays of 20–50 ps and 1–2 pJ delay–dissipation products can be achieved. In most of these cases, the device low-field resistance was of the order of 300–1000 Ω. Hartnagel [5] has shown that a load resistance (R_L) value of 1–1.5 times the device low-field resistance is necessary to develop an output voltage which is of the same magnitude as the input trigger voltage. Mause *et al.* [6] have pointed out that if such high load resistances are used, the propagation delay and rise time of the signals will be limited by the external circuit charging time constants (R_LC) rather than the intrinsic domain formation times (5–15 ps). The value of the total input capacitance (i.e., capacitance of the interconnect lines + input capacitance of the following gates) thus significantly degrades device performance. Unless the interconnections are made on the chip itself [7], [8], the total input capacitance is large and use of devices with large low-field resistance should be avoided.

Sugeta *et al.* [9] and Mause *et al.* [6] have presented TELD design procedures. In these designs, the transit length is fixed by the desired frequency of operation. The device width is then chosen to minimize the dc dissipation. Devices fabricated following these procedures generally have large low-field resistances leading to extrinsic constraints on device speed. Furthermore, a recent study by Upadhyayula [10] has shown that it is desirable to design TELD's with a reasonable high subthreshold transconductance (g_m) since it improves the trigger sensitivity by $(1 + g_mR_L)$ and increases the device voltage gain by g_mR_L. It is well known from classical FET theory that g_m is proportional to the ratio of the channel width (W) to the gate length (l_g) [11]. This design criterion therefore sets a limit to decreasing W in order to minimize power dissipation. We have now developed a design procedure which results in improved transconductance by optimizing the ratio W/l_g, and keeps device dissipation within tolerable limits by decreasing the transit length l_t. This also results in a device low-field resistance of 50–75 Ω and allows the use of 100-Ω load resistors. It is relatively easy to obtain transmission lines of such a characteristic impedance, making device interconnection simpler. This paper will discuss our design procedure and present some experimental results.

II. Device Design

A three-terminal TELD is schematically shown in Fig. 1. A proper choice of the device geometry (i.e., dimensions) and material parameters has to be made for good device performance. We will now discuss some of the important device parameters and show how they are related to the material characteristics and device dimensions. Based on this discussion, we will outline a design procedure for optimum device performance. The parameters that play an important role in device performance are: 1) trigger sensitivity (ΔV_g), 2) voltage gain (G_V) or fanout, 3) propagation delay (τ_D), and 4) delay-dissipation product.

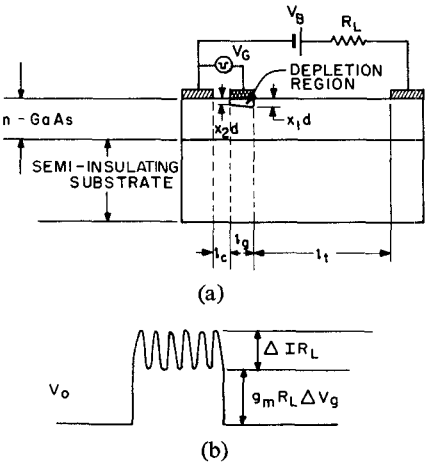


Fig. 1. (a) Schematic of device structure. (b) Output voltage V_o for a wide input pulse.

A. Trigger Sensitivity Considerations

The minimum trigger voltage (ΔV_g) required for nucleating domains in a TELD is given by [10]

$$\Delta V_g \leq \frac{0.2x_{1th}(1 - x_{1th})\phi_p}{(1 + g_mR_L)} \tag{1}$$

or

$$\Delta V_g = \frac{0.2\phi}{(1 + g_mR_L)}\left(\frac{1}{x_{1th}} - 1\right) \tag{2}$$

where

- ϕ reverse bias on the Schottky gate;
- ϕ_p pinchoff voltage;
- x_{1th} depletion layer thickness at the anode edge of the Schottky gate normalized to the active layer thickness (d).

The built-in diffusion potential for GaAs Schottky barriers (ϕ_b) is about 0.8 V. Standard photolithographic techniques used in the device fabrication will limit l_{cg} = 1–2 μm and l_g = 2.0 μm. Therefore, for most of the practical devices $\phi \simeq 2.0$ V. The trigger sensitivity curve for ϕ = 2.0 V from [10] is reproduced in Fig. 2. g_mR_L represents the voltage gain of the device for below-threshold operation. The trigger sensitivity increases by a factor $(1 + g_mR_L)$ when the device has a good low field g_m. As shown in Section II-B, g_mR_L typically lies between 0.25 and 1.0. The trigger sensitivity for practical devices therefore lies between the two curves of Fig. 2. A desirable value for trigger sensitivity (ΔV_g) is between 0.5 and 1.5 V. This corresponds to a pinchoff voltage ϕ_p of 22–50 V. It has been established from domain dynamics that $nd \geq 10^{12}$ cm^{-2} and $nl \geq 10^{13}$ cm^{-2} where n is the doping density, d is the channel thickness, and l is the transit length [6].

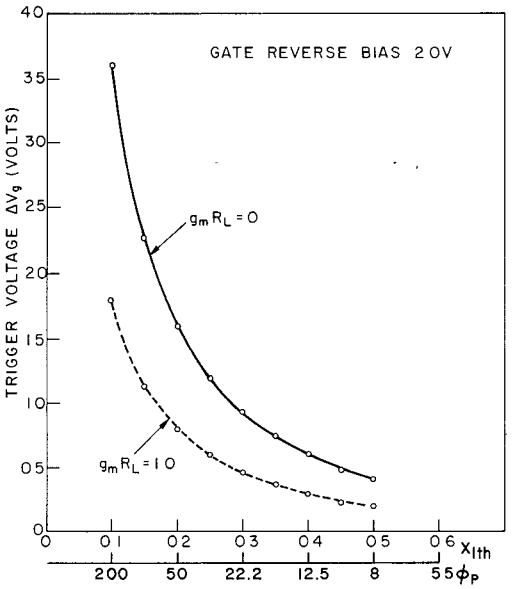


Fig. 2. Trigger sensitivity of a TELD as a function of fractional depletion width (x_{1th}) or pinchoff voltage (ϕ_p) for $\phi = 2.0$ V. nd is kept constant and both n and d are allowed to vary. g_mR_L is used as a parameter.

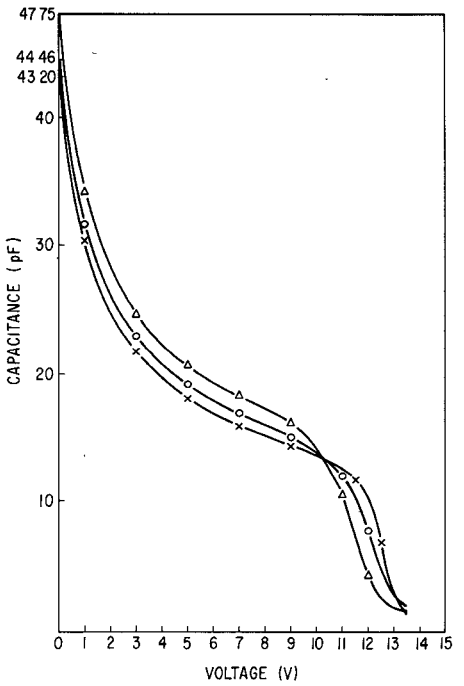


Fig. 3. Schottky-barrier capacitance of typical test diodes as a function of reverse-bias voltage.

TABLE I

ϕ_p	$nd = 2\times10^{12}$ cm^{-2}		$nd = 4\times10^{12}$ cm^{-2}	
	$n(\times10^{16}$ cm$^{-3})$	d(μm)	$n(\times10^{16}$ cm$^{-3})$	d(μm)
22.0 V	1.3	1.54	5.2	0.77
50.0 V	0.6	3.5	2.9	1.75

Table I shows the doping density and channel thickness for $nd \simeq 2 \times 10^{12}$ cm^{-2} and 4×10^{12} cm^{-2}. From Table I it is evident that the doping density should range from 0.6 to 5.2×10^{16} cm^{-3} and the n-layer thickness should range from 0.77 to 3.5 μm.

B. Below-Threshold Transconductance (g_m)

When biased below threshold field, a TELD operates in a manner similar to a Schottky gate or junction FET. From Bockemuehl's analysis [11] on JFET's, g_m is given by

$$g_m = \frac{W}{l_g} ne\mu d[x_{1th} - x_{2th}] \tag{3}$$

where $ne\mu = \sigma$ and the other parameters have been defined with reference to Fig. 3. If standard photolithographic techniques are used in the device fabrication, $l_{cg} \simeq 1$–2 μm and $l_g \simeq 2.0$ μm. For Schottky barriers on GaAs the built-in potential (ϕ_b) $\simeq$ 0.8–1.0 V. If the material parameters are selected such that $nd \simeq 2 \times 10^{12}$ cm^{-2} with $n \simeq 2 \times 10^{16}$ cm^{-3} and $\mu \simeq$ 5000–5500 cm^2/V · s, g_m can be computed from (3) for any W/l_g ratio. The transconductance (g_m) can be shown to be 5 m · mhos for $W/l_g = 50$ and 10 m · mhos for $W/l_g \simeq 100$. The device low-field resistance turns out to be in the 30–70-Ω range which allows load resistance (R_L) values of about 100 Ω. For R_L of 50–100 Ω and g_m of 5–10 m · mhos, we obtain g_mR_L values of 0.25–1. This explains our choice of g_mR_L values of 0 and 1 in Fig. 2. It should be noted that conventional high-speed logic such as emitter-coupled logic (ECL) and transistor–transistor-coupled logic (TTL) use load resistance values of the order of 50 and 100 Ω.[1] It is appropriate to use similar load resistors with TELD's also so that they will be compatible with the standard logic families.

C. Voltage Gain of a TELD

The output voltage (V_o) of a TELD is a square pulse with the transit time oscillations superimposed on the top of it as shown in Fig. 1(b). The amplitude of the pedestal is equal to $g_mR_L\Delta V_g$, and the amplitude of the oscillation is equal to ΔIR_L, where ΔI is the current dropback when the device thresholds. The voltage gain (G_v) is therefore given by [10]

$$G_v = (g_mR_L\Delta V_g + \Delta IR_L)/\Delta V_g. \tag{4}$$

Sugeta *et al.* [9] have pointed out that $\Delta I \simeq 0.2$–$0.3I_{th}$ for $x_{1th} \approx 0.2$–0.3. Hence

$$G_v \geq \left(g_m + \frac{0.2I_{th}}{\Delta V_g}\right) R_L. \tag{5}$$

As shown in the previous section, $g_m \simeq 5$–10 m · mhos are feasible. For $I_{th} \simeq$ 25–50 mA, voltage gain greater than 1.0 can be realized with $R_L =$ 50–100. Notice that when g_m is small, either I_{th} or R_L has to be increased by a factor of almost 2.0 to obtain voltage gain of unity or more.

[1] MECL system design handbook, Motorola Semiconductor Products, Inc.

D. Power Dissipation

In the depletion mode of operation, the TELD dissipates a dc power of $0.9\text{–}0.95V_{th}I_{th}$ [6] in the standoff condition. The dc dissipation in the fastest commercially available logic gates (ECL) is 60–100 mW. Therefore, a design goal of 100–150-mW dissipation per TELD gate is not unreasonable in view of its order of magnitude lower propagation delay. Since the threshold current from voltage gain point of view is fixed at 25–50 mA assuming a load resistor of 100 Ω, the threshold bias has to be 3.0–6.0 V. Since the threshold electric field for GaAs devices at room temperature is about 3.2 kV/cm, the cathode-to-anode spacing turns out to be 9.5–19 μm for power dissipation of 100–150 mW.

E. Propagation Delay

The domain formation time for the values of doping density considered herein is of the order of 5–15 ps. When external charging time constants do not limit the device performance, the propagation delay in a TELD is approximately equal to the domain formation time.

The device design parameters generated are now summarized as follows:

Cathode–anode spacing (l_{ca})	$\simeq$ 10–20 μm
Cathode–gate spacing (l_{cg})	= 1–2 μm
Gate length (l_g)	$\simeq$ 2 μm
Gate width (W)	= 120–200 μm
Doping density	$\simeq$ 1–4 × 10^{16} cm^{-3}
Channel thickness	$\simeq$ 0.8–3.5 μm
Trigger sensitivity	$\simeq$ 0.5–1.0 V
Voltage gain	$\simeq$ 1–1.2.

III. Device Fabrication

Epitaxially grown GaAs n-layers on semiinsulating substrates 3° off the (100) plane were used for device fabrication. The n-layers were doped with sulfur to the required carrier density. Chrome-doped buffer layers were also used in some of the wafers to minimize the problems associated with the epi–substrate interface. The wafers were thinned by a process of anodic oxidation and oxide stripping as discussed by Rode *et al.* [12]. This self-limiting electrolytic process tailors the wafer thickness such that the *nd* product (not *d*) across the wafer is constant. The uniformity of *nd* product in the electrolytically etched GaAs wafers has been confirmed from the *C–V* measurements. Fig. 3 shows the *C–V* plots on a typical device wafer. The *nd* product in the wafer is given by

$$nd = \frac{Q}{Ae} = \frac{\text{area under the curve}}{Ae}$$

where A is the cross-sectional area of the Schottky diode and e is the electronic charge. From Fig. 3 the *nd* product in this wafer is $3.0 \pm 0.3 \times 10^{12}$ cm^{-2}.

Multilevel mesa-type devices were fabricated using standard photolithographic techniques. Ohmic contacts were made by vacuum depositing AuGe/Ni/Au and sintering. Cr/Au was vacuum deposited for Schottky-barrier gates. A photomicrograph of a fabricated device is shown in Fig. 4(a). The device dimensions are: $l_{ca} = 12$ μm, $l_{cg} \simeq 1$ μm, $l_g \simeq 2$ μm, and $W_{av} = 120$ μm. The ratio of the channel width at anode to that at the cathode is 1.2.

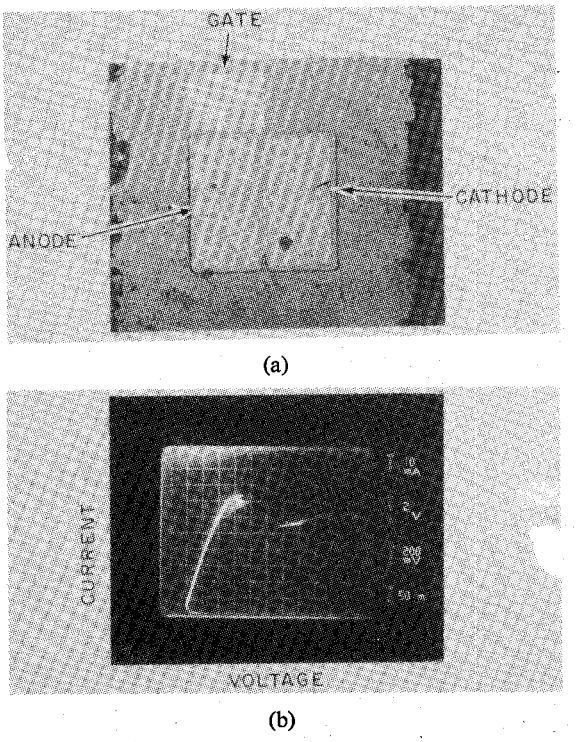


Fig. 4. (a) Photomicrographs of fabricated multilevel mesa devices. (b) *I–V* characteristics.

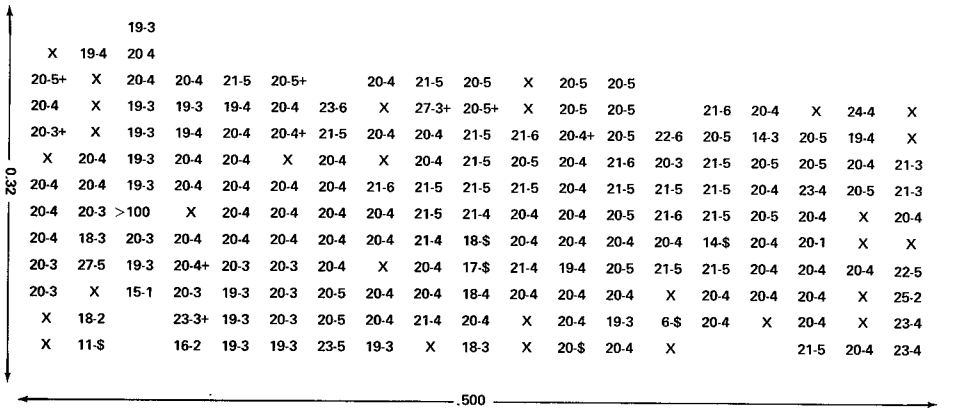
IV. Device Evaluation

The *I–V* characteristic of a typical device is shown in Fig. 4(b). The threshold current for this device is 70 mA with 15-mA current dropback and 6.0-V threshold bias. The minimum trigger signal required at the gate for threshold is −1.0 V. Even though the ohmic contacts were symmetrical and truly ohmic, the threshold bias is higher than the theoretical value. These devices were fabricated from a GaAs wafer with n-layers on semiinsulating substrate and did not have any buffer layer. The tapered channel and/or presence of trapping centers at the epi–substrate interface [13] may be responsible for the higher threshold voltage. The threshold current and current drop were measured on every device in a wafer. Fig. 5 shows the data on a particular wafer. The variation in the threshold current and current drop is less than 10 percent across a 0.35 × 0.45-in wafer. This good uniformity is due to the electrolytic etching of the wafer which resulted in constant *nd* across the wafer.

A. Threshold Gate

Single-input logic gates, cascaded two-stage logic gates, and a two-input AND gate were fabricated and their performance studied. The threshold switching characteristic, transit time behavior, and the capability to process picosecond-width pulses were investigated.

A single-stage TELG is shown in Fig. 6(a). An anode load resistor (R_L) of about 100 Ω was used. The threshold switching characteristic of this logic gate is shown in Fig.



		19-3																
X	19-4	20 4																
20-5+	X	20-4	20-4	21-5	20-5+		20-4	21-5	20-5	X	20-5	20-5						
20-4	X	19-3	19-3	19-4	20-4	23-6	X	27-3+	20-5+	X	20-5	20-5		21-6	20-4	X	24-4	X
20-3+	X	19-3	19-4	20-4	20-4+	21-5	20-4	20-4	21-5	21-6	20-4+	20-5	22-6	20-5	14-3	20-5	19-4	X
X	20-4	19-3	20-4	20-4	X	20-4	X	20-4	21-5	20-5	20-4	21-6	20-3	21-5	20-5	20-5	20-4	21-3
20-4	20-4	19-3	20-4	20-4	20-4	20-4	21-6	21-5	21-5	21-5	20-4	21-5	21-5	21-5	20-4	23-4	20-5	21-3
20-4	20-3	>100	X	20-4	20-4	20-4	20-4	21-5	21-4	20-4	20-4	20-5	21-6	21-5	20-5	20-4	X	20-4
20-4	18-3	20-3	20-4	20-4	20-4	20-4	20-4	21-4	18-$	20-4	20-4	20-4	20-4	14-$	20-4	20-1	X	X
20-3	27-5	19-3	20-4+	20-3	20-3	20-4	X	20-4	17-$	21-4	19-4	20-5	21-5	21-5	20-4	20-4	20-4	22-5
20-3	X	15-1	20-3	19-3	20-3	20-5	20-4	20-4	18-4	20-4	20-4	20-4	X	20-4	20-4	20-4	X	25-2
X	18-2		23-3+	19-3	20-3	20-5	20-4	21-4	20-4	X	20-4	19-3	6-$	20-4	X	20-4	X	23-4
X	11-$		16-2	19-3	19-3	23-5	19-3	X	18-3	X	20-$	20-4	X			21-5	20-4	23-4

Fig. 5. Map of threshold current and current drop of a typical wafer. These measurements were made on 35-μm channel (l_{ca}) devices. This wafer also contained chrome-doped buffer layer.

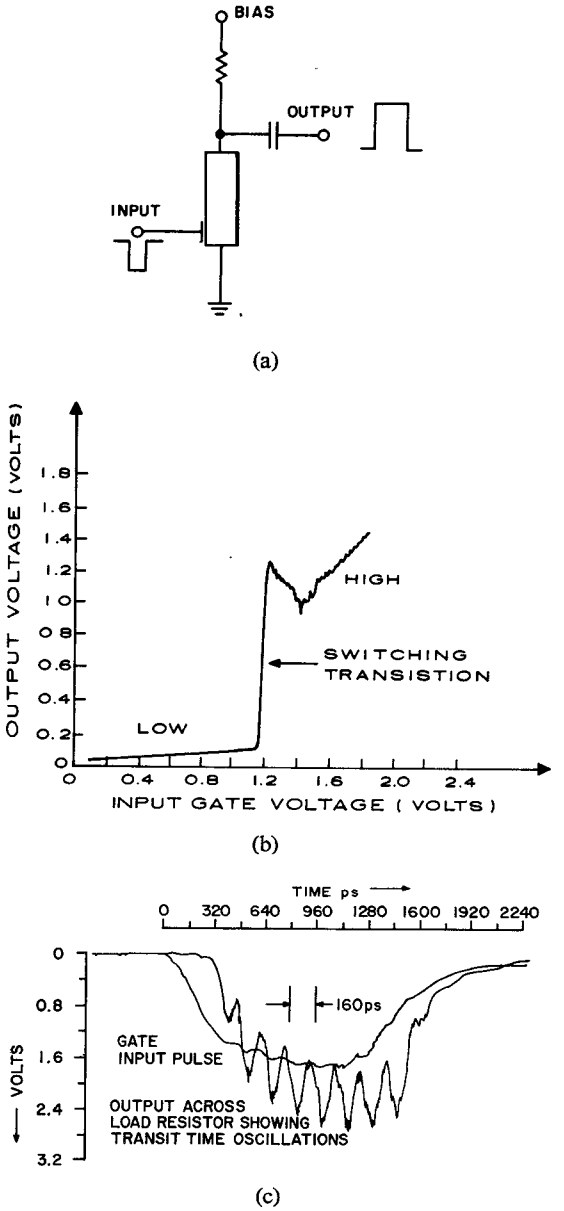


Fig. 6. (a) Schematic of a TEDG. (b) Threshold switching characteristics of a TELD. (c) Performance of a typical TELD fabricated according to new design guidelines

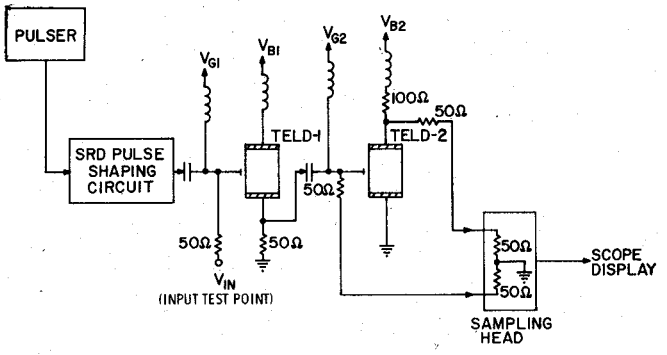
6(b). For input voltage less than 1.2 V the output remained below 0.2 V, and for input voltage greater than 1.2 V the output rose to above 1.2 V. The switching transition occurred within 50–80 mV. The response of this logic gate to a wide input pulse is shown in Fig. 6(c). Notice that the output amplitude is larger than the input (i.e., voltage gain is greater than 1.0) and the output waveform shows periodic oscillations with 160-ps period. Near transit time oscillations are characteristic of transferred electron devices. A cascaded two-stage logic gate circuit is schematically shown in Fig. 7(a). TELD-1 has a cathode load resistor and produces a negative polarity output when a negative input pulse is applied at its gate. The output of TELD-1 is used to trigger TELD-2. TELD-2 has a load resistor in the anode and produces a positive output pulse. The leading and trailing edges of the output of a charge-line pulser were shaped using step recovery diode (SRD) pulse shaping circuit and used as input to TELD-1. Fig. 7(b) shows the response of the cascaded gate circuit when the input to TELD-1 exceeds the threshold value. Note that outputs of both TELD-1 and TELD-2 are high, indicating TELD-1 has enough output to trigger TELD-2. The output pulses are less than 100 ps wide at half-height and correspond to single-domain transit time in these devices.

B. Propagation Delay

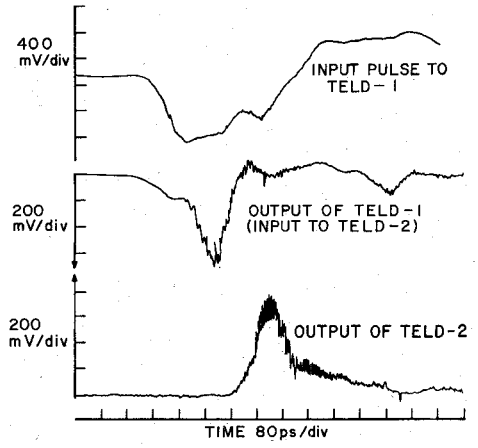
The propagation delays in TELD's were measured on devices fabricated according to earlier designs. These devices had 35-μm transit length and about 300-Ω low-field resistance. The measured propagation delay was of the order of 20–50 ps.

C. Two-Input AND Gate

A two-input AND circuit was fabricated using TELD's. A resistive summing network and a threshold gate formed the AND circuit. The two-input pulses to the AND gate were also derived from two TELD gates. This test circuit is shown schematically in Fig. 8. A charge-line pulser provided single pulses less than 500 ps wide and double pulses less than 800-ps separation for testing the circuit. A resistive divider was used to feed the input pulses to the



(a)



(b)

Fig. 7. (a) Schematic of cascaded two-stage circuit used to show that output of one TELD can trigger another (b) Performance of the cascaded two-stage TELD circuit for input pulses above threshold.

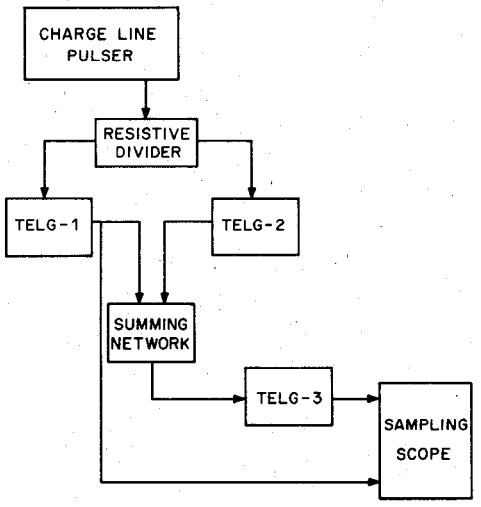


Fig. 8. Schematic of AND circuit.

two TELD gates. The electrical path length to one of the gates was varied with respect to the other by a known amount. The performance of the AND circuit is shown in Figs. 9–11. The output of the AND circuit is present only when both the inputs to the gates are present simultaneously (Fig. 9). The AND circuit output is zero when the two-input pulses are separated by about 500–600 ps. The output of

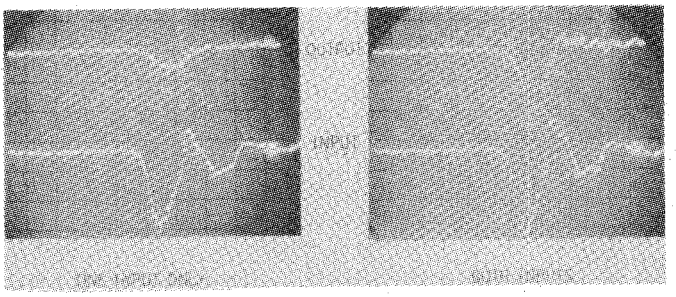
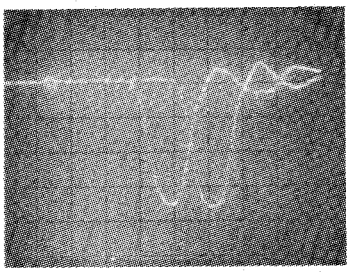
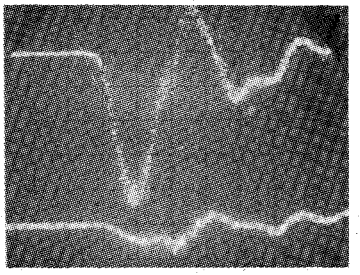


Fig. 9. Performance of the AND circuit for a single-pulse input when the electrical paths to the two TELD gates are equal. The output of the AND circuit along with one of the inputs is shown here. Horizontal scale: 500 ps/div. Vertical scale: input—180 mV/div; output—100 mV/div.



(a)



(b)

Fig. 10. Performance of the AND circuit when the two inputs are separated by about 600 ps. The output of the AND circuit along with the inputs to the two TELD gates and the output of one of the two TELD gates is shown here. The output of the AND circuit is "0" as the outputs of the two gates are not in coincidence. (a) Input. (b) Output.

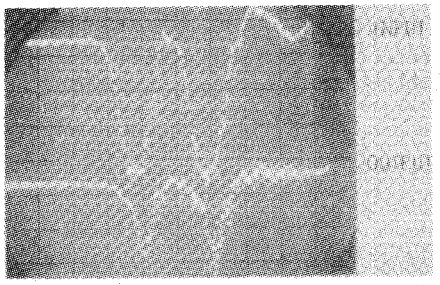


Fig. 11. Performance of the AND circuit for a double-pulse input. Bottom trace: output 100 mV/div. Top trace: input 180 mV/div. Time base 500 ps/div.

the AND circuit for double-pulse input is shown in Fig. 11. The double-pulse input was fed to both the TELD gates simultaneously. The AND circuit performed satisfactorily. The 800-ps resolution time measured here is not the limit of the AND circuit, but that of the test instrumentation.

V. Summary and Conclusions

A new design procedure has been outlined for TELD's which results in improved performance. An electrolytic etch thinning process has been used to maintain uniform *nd* product across the wafers. Devices fabricated from these wafers showed less than 10-percent variation in their characteristics. These devices were tested in standard logic gate circuits. The trigger sensitivity of these devices is about 1.2 V with propagation delay less than 50 ps. These data agree closely with the design goals. Logic gates have been operated in cascaded configuration. The below-threshold transconductance of the fabricated devices is smaller ($\approx$ 2 m · mhos) than desired ($\approx$ 5 m · mhos) and the dc dissipation is higher ($\simeq$ 250 mW). These differences are due to higher doping density than desired and consequently higher device *nd* product.

Acknowledgment

The authors wish to thank Dr. F. Sterzer and Dr. S. Y. Narayan for many helpful technical discussions and J. E. Brown for his help in the fabrication of the circuits.

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Multiplexing and Demultiplexing Techniques with Gunn Devices in the Gigabit-per-Second Range

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Abstract—**In this paper a circuit is described which can process signals in the gigabit-per-second range for fast PCM applications. Such circuits will be interesting for future communication links, especially in connection with glass fibers. A monolithically integrated shift register with Gunn devices on GaAs is used. A circuit consisting of five stages is described and experimental results for bit rates near 2 Gbit/s are reported.**

Introduction

MONOMODE glass fiber transmission lines are believed to be able to transmit bit rates up to some gigabits per second. It is believed that this range will become interesting for future PCM transmission applications. To process signals for such fast time multiplexing systems, multiplexing and demultiplexing circuits are needed. Up to this date the realization of fast circuits operating above 1 Gbit/s in silicon technique was not very successful. There seems to exist a limit around 1 Gbit/s for monolithically integrated bipolar circuits.

This paper describes a dynamic shift register as an example of circuit integration with Gunn devices, the technique of which offers advantages in the range above 1 Gbit/s. The complex performance of Gunn devices carrying high-field domains makes possible a variety of logic operations which can be carried out in one device [1], [2]. Further merits are the steep ramps of the pulses generated [3], the small delay between subsequent stages [4], and the automatic regeneration of the pulse shape within the circuit. In most cases these properties of Gunn devices result in a considerable simplification of the circuit design as compared to circuits with bipolar transistors or field-effect transistors. Additionally, planar devices on semiinsulating GaAs

Manuscript received May 14, 1976; revised July 23, 1976.
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